800G OSFP-RHS SR8 Transceiver, MMF 8×100G PAM4 850nm, 100M

Features

- Data Rate 106.25 Gb/s PAM4 per lane
- Digital Diagnostics Monitoring Interface
- Reach up to 100m over MMF(OM4)
- Hot-pluggable OSFP form factor
- 850nm VCSEL laser and PIN receiver
- Commercial operating case temperature range: 0~ 70ºC
- MPO-16 APC or 2xMPO-12 APC connector
- RoHS-6 compliant
- TDECQ< 4.4dB
- Single 3.3V power supply
- Power dissipation <14W
- IEEE Std 802.3df
- 800G OSFP-RHS SR8 MSA and CMIS 5.1

Application

- 800G SR8
- Data center networks
- InfiniBand NDR applications

Ordering Information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX	Sen (dBm)	Temp (℃)	Reach (M)	DDM
ELOM800G-OSFP-SR8-S	OSFP-RHS	800G	850 VCSEL	-4.6~4	Pin	＜-6.4	0~70	100	Y

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Ambient Temperature	T_{STG}	-40	85	℃
Operating Humidity	H_O	5	85	%
Power Supply Voltage	Vcc	-0.3	3.6	V
Signal Input Voltage		Vcc-0.3	Vcc +0.3	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		70	℃
Power Supply Voltage	Vcc	3.13	3.3	3.47	V
Data Rate, each Lane（PAM4）			106.25		Gbps
Fiber Length 50/125μm core MMF		-	-	100	m

Electrical Power Supply Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit	Notes
Data Rate per lane	DR	-	106.25 53.125	-	Gbps GBd	Each Lane PAM4
Transmitter						
Single Ended Output Voltage Tolerance		-0.3	-	4.0	V	
Common mode voltage tolerance		15	-	-	mV	
Input differential impedance	Rin	-	100	-	Ω	
Differential Input Voltage swing	Vin	300	-	1100	mV	
Tx Fault	VoL	-0.3		0.4	V	At 0.7mA
Receiver						
Single Ended Output Voltage Tolerance		-0.3	-	4.0	V	
Differential Output Swing	Vout	300	-	900	mV	
Output differential impedance	Rout		100		Ω	

Optical Characteristics

Optical transmitter Characteristics						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Launched Power (avg.) Per Lane	Pavg	-4.6		4	dBm	
Wavelength Range	λ0	844	850	863	nm	
Spectral Width(-20dB)	Δλ			0.6	nm	
Extinction Ratio	ER	2.5			dB	
Transmitter OFF Output Power	POff			-30	dBm	
Optical Modulation	OMA	-2.6		3.5	dBm	

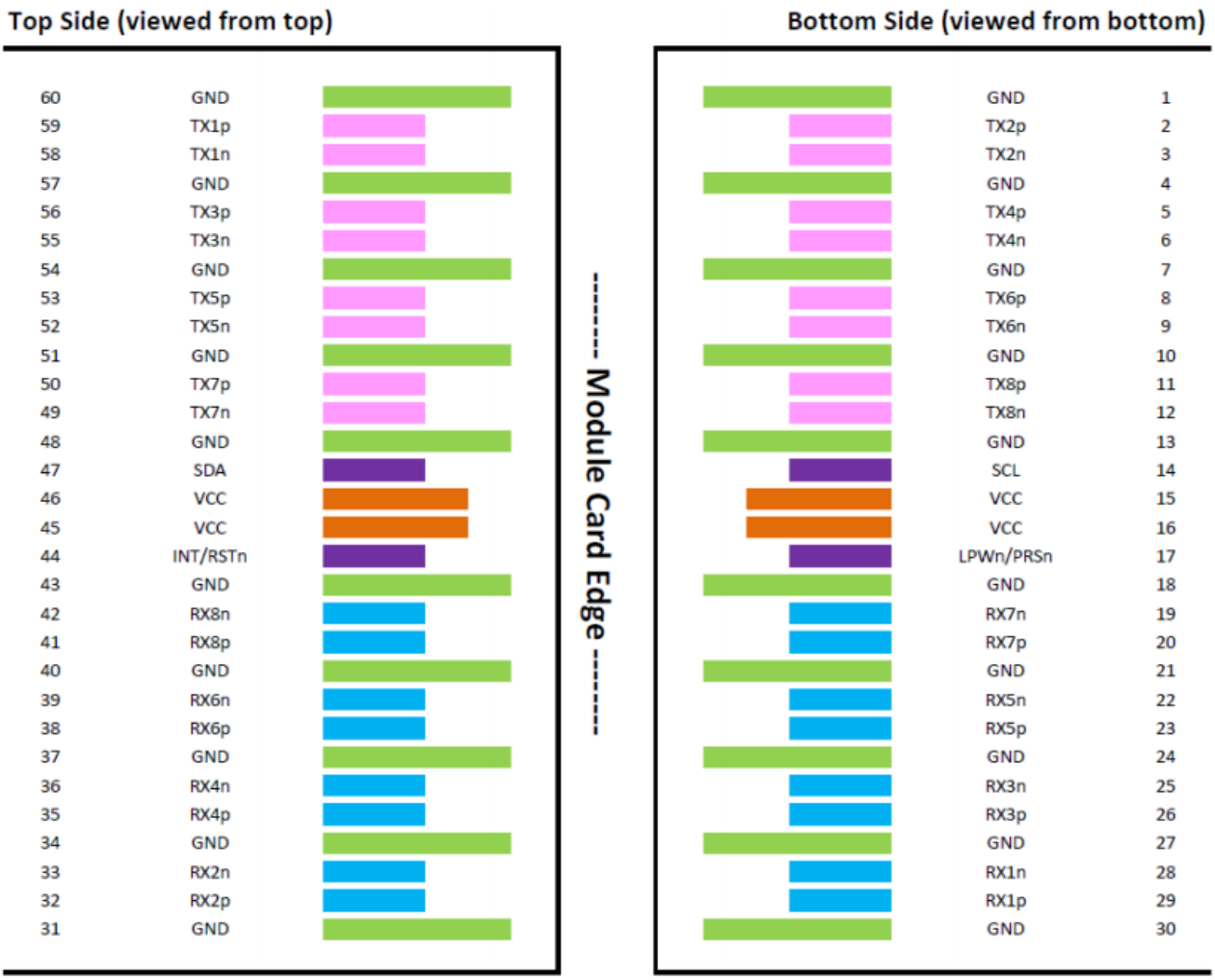
Amplitude(OMA outer)						
Transmitter and dispersion eye closure(TDECQ)	TDECQ			4.4	dB	

Optical receiver Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Receiver Wavelength Range		844	850	863	nm	
Average Receiver Power Per Lane		-6.4		4	dBm	
Receiver Sensitivity（OMAouter） Max(TECQ, TDECQ) ≤1.8dB 1.8<max(TECQ, TDECQ) ≤4.4dB	PSen			(-4.6, -6.4+TECQ)	dBm	1
Optical Power Input Overload	P_{in-max}	3.5			dBm	
Receiver Reflectance	Rr			-12	dB	

Notes:

1. BER=2.4E-4; PRBS31Q@53.125GBd.
2. if max (TECQ, TDECQ) ≤ 1.8dB, the OMA (min) = -2.6; if 1.8 < max (TECQ, TDECQ) ≤ 4.4dB, the OMA (min) = -4.4 + max (TECQ, TDECQ).

Pin Definition



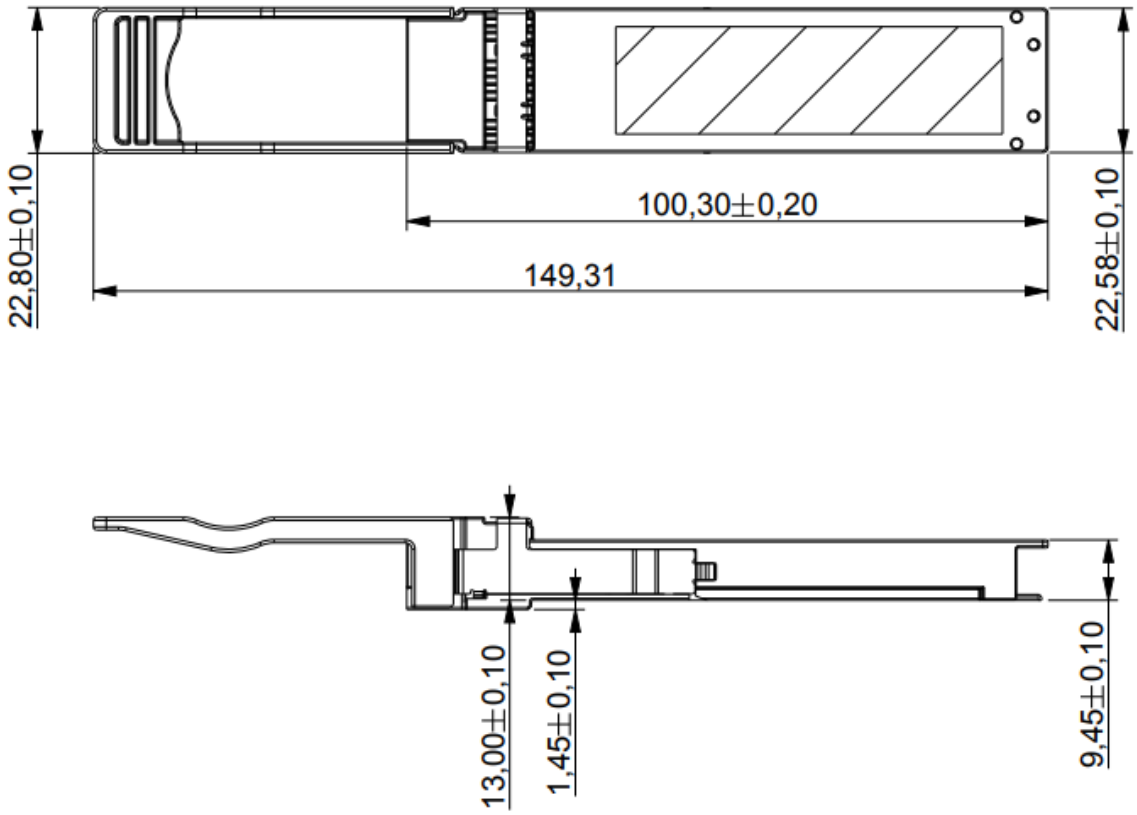
OSFP MSA-compliant 60-pin connector

The INT/RSTn signal operates in three voltage zones to indicate the Reset state for the module and Interrupt state for the host. The host uses a 2.5 V reference to determine H_INT, while the module uses a 1.25 V reference to determine M_RSTn.

Pin	Signal	Description	Logic	Direction	Pin Type	Remarks
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS- I/O	Bi-directional	3	Open-Drain with pull up resistor on H
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
33	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
36	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
39	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
42	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS- I/O	Bi-directional	3	Open-Drain with pull up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

OSFP Module PIN Definition

Package Outline



Regulatory Compliance

Feature	Test	Method
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1(>1000V for SFI pins, >2000Vfor other pins.)
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2:2025	Test level per applicable product/system requirement
Electromagnetic Interference (EMI)	CISPR 32:2015 + AMD1:2019	Class B*
Immunity	IEC61000-4-3	Comply with standard
Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Compatible with Class I laser Product
Environmental	RoHS Directive 2011/65/EU + (EU) 2015/863 REACH Regulation (EC) No. 1907/2006	RoHS and REACH compliant*

Compliance classification is subject to final product qualification and applicable test reports.